CLAIMS

1. Shift register containing a plurality of cascaded stages, each stage being connected up to two clock signals, containing an output and characterized in that it is connected moreover to the output of the preceding stage and to the output of the next stage, and that it includes a first semiconductor output device switching the associated output between high and low values of a first clock signal, this first semiconductor device being controlled by the potential of a first node connected:

- to the output of the preceding stage across a second semiconductor device controlled by this same preceding output,
- to a negative potential across a third semiconductor device controlled by the output of the next stage,
- to a second clock signal across a first capacitance,
- and to the output associated with the stage across a second capacitance.

2. Shift register containing a plurality of cascaded stages, each stage being connected up to two clock signals containing an output and characterized in that it is connected moreover to the output of the preceding stage, and to the output of the next stage, and that it includes a first semiconductor output device switching the associated output between high and low values of a first clock signal, this first semiconductor device being controlled by the potential of a first node connected:

- to the output of the preceding stage across a second semiconductor device controlled by this same preceding output,

- to a second clock signal (Φ2) across a first capacitance (Cc),
- to the output (D) associated with the stage (J) across a second capacitance (Cb), the said output being connected to earth (33) across a third semiconductor device (Tz) controlled by a second node (Z),
- and to earth across a fourth semiconductor device (Td) controlled by the second node (Z),

this second node (Z) being connected moreover:

- to the output (22) of the preceding stage (J-1) across a fourth capacitance (Cc),
- to earth across a fifth semiconductor device (Tr) controlled by the output (22) of the preceding stage (J-1),
- to the output (30) of the next stage (J+1) across sixth and seventh clamping transistors (Th, Tg) mounted in parallel and controlled, one by the second node (Z) and the other by the output (30) of the next stage (J+1),
- and to that terminal of the third semiconductor device (Tz) connected to earth (33), by a capacitance (Cg).

3. Shift register (55) containing a plurality of cascaded stages (J-1, J, J+1), each stage (J) being connected up to two clock signals (Φ1, Φ2) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1) or of the next but one stage (J+2), the said stage (J) including a first semiconductor output device (T1) switching the associated selection line (J) between high and low values of a first clock signal (Φ1), this first semiconductor device (T1) being controlled by the potential of a first node (G) connected:

- to the output of the preceding stage (J-1) across a second semiconductor device (Tp) controlled by this same preceding output (22),

- to a second clock signal (Φ2) across a first capacitance (C2),
- to the output (D) associated with the stage (J) across a second capacitance (Cb), the said output (D) being connected to earth (32) across a fourth semiconductor device (Tz) controlled by a second node (Z),
- to a negative potential (V-) across a third semiconductor device (Td) controlled by the second node (Z) which is moreover connected to the output (30) of the next stage (J+1) or of the next but one stage (J+2).

4. Shift register (21) containing a plurality of cascaded stages (J-1, J, J+1), each stage (J) being connected up to two clock signals (Φ1, Φ2) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1), and that it includes a first semiconductor output device (T1) switching the associated output (J) between high and low values of a first clock signal (Φ1), this first semiconductor device (T1) being controlled by the potential of a first node (G) connected:

- to the output (22) of the preceding stage (J-1) across a second semiconductor device (Tp) controlled by this same preceding output (22),
- to a signal (V) across a third semiconductor device (Td) controlled by the output of the next stage (J+1),
- to a second clock signal (Φ2) across a first capacitance (C2),
- and to the output (D) associated with the stage (J) across a second capacitance (Cb), this output (D) being connected to earth across a fourth semiconductor device (Tz) controlled by a zero-reset signal.

5. Shift register (21) containing a plurality of cascaded stages (J-1, J, J+1), each stage (J) being

connected up to two clock signals (Φ1, Φ2) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1), and that it includes a first semiconductor output device (T1) switching the associated output (J) between high and low values of a first clock signal (Φ1), this first semiconductor device (T1) being controlled by the potential of a first node (G) connected:

- to the output (22) of the preceding stage (J-1) across a second semiconductor device (Tp) controlled by this same preceding output (22),
- to a constant negative potential (V-) across a third semiconductor device (Td) controlled by a clock signal (Φa) chosen from three clock signals (Φa, Φb, Φc) [lacuna] the output of the next stage (J+1),
- to a second clock signal (Φ2) across a first capacitance (C2),
- and to the output (D) associated with the stage (J) across a second capacitance (Cb), this output (D) being connected to earth across a fourth semiconductor device (Tz) controlled by a zero-reset signal.

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6. Shift register according to ~~the preceding claim~~ Claim 5, characterized in that each of the clocks (Φa, Φb, Φc) consists of short pulse (T3) lagging behind the transitions of the first (Φ1) and second (Φ2) clock signals.

7. Shift register according to ~~any one of the preceding claims~~ Claim 1, characterized in that the first (Φ1) and second (Φ2) clock signals are complementary.

8. Shift register according to ~~any one of the preceding claims~~ Claim 1, characterized in that the first capacitance (C2) has a value slightly greater than the value of the stray capacitance (Cp) of the semiconductor output device (T1).

9. Shift register according to ~~any one of claims 1 to 7~~ Claim 1, characterized in that the first capacitance (C2)

has a value slightly less than the value of the stray capacitance (Cp) of the semiconductor output device (T1).

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10. Shift register according to claim 8 ~~or 9~~, characterized in that the second capacitance (Cb) has a value substantially greater to that of the stray capacitance (Cp) of the semiconductor output device (T1).

11. Shift register according to Claim 1 ~~any one of the preceding claims~~, characterized in that the semiconductor devices (T1, Tp, Td, Tz, Tr, Th) are amorphous silicon transistors.

12. Shift register according to Claim 1 ~~any one of the preceding claims~~, characterized in that the outputs (D, 22, 30) of the stages (J-1, J, J+1) are lines for addressing an active matrix of a liquid crystal screen.

13. Viewing screen containing integrated peripheral control circuits made up of selection line scanners and column scanners, characterized in that at least one of these circuits includes a shift register according to Claim 1 ~~any one of the preceding claims~~.

14. Viewing screen including peripheral control circuits, integrated with or external to the substrate board on which the active matrix is deposited, and which are made up of scanners (Dj-1, Dj, Dj+1) for selection lines (j-1,,j,,j+1) and of scanners for columns (i-1 , i, i+1), characterized in that it furthermore includes a supplementary conductive column (f) crossing over the selection lines (j-1,,j,,j+1) and capacitively coupled (Cfi) to each of them in such a way that corresponding coupling capacitances (Cfi) each have a value close to the sum of the coupling capacitances (Cij) between a line (j) and the columns which it crosses (i-1 , i, i+1).

15. Viewing screen according to Claim 14 ~~the preceding claim~~, characterized in that associated with this supplementary conductive column (f) is a supplementary conductive line (g) capacitively coupled (Cfg) with it

and associated with it across a comparator circuit (40), this supplementary line (g) being coupled capacitively to each of the columns (i-1, i, i+1).

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16. Viewing screen according to ~~either one of~~ claims 14 ~~and 15,~~ characterized in that it includes one or more shift registers according to ~~any one of claims 1 to 12~~ Claim 1 as well as the supplementary lines and columns according to ~~either one of~~ claims 14 ~~and 15~~.